FIG. 1

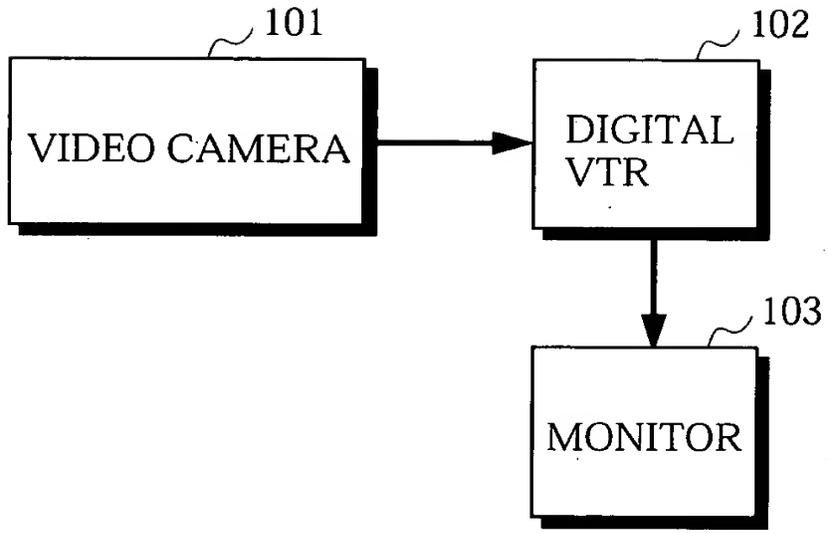


FIG. 2

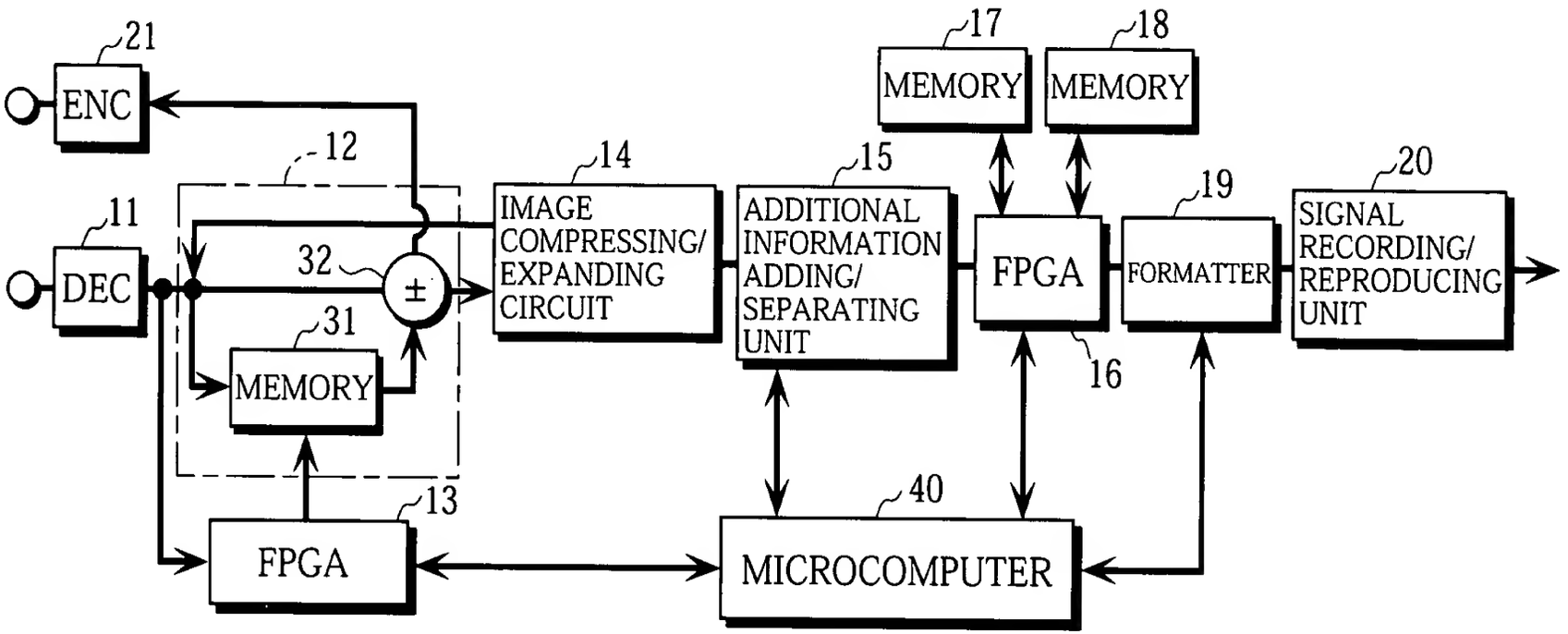

21
ENC
11
DEC
12
32
±
31
MEMORY
13
FPGA
14
IMAGE COMPRESSING/ EXPANDING CIRCUIT
15
ADDITIONAL INFORMATION ADDING/ SEPARATING UNIT
17
MEMORY
18
MEMORY
FPGA
16
19
FORMATTER
20
SIGNAL RECORDING/ REPRODUCING UNIT
40
MICROCOMPUTER

FIG. 3

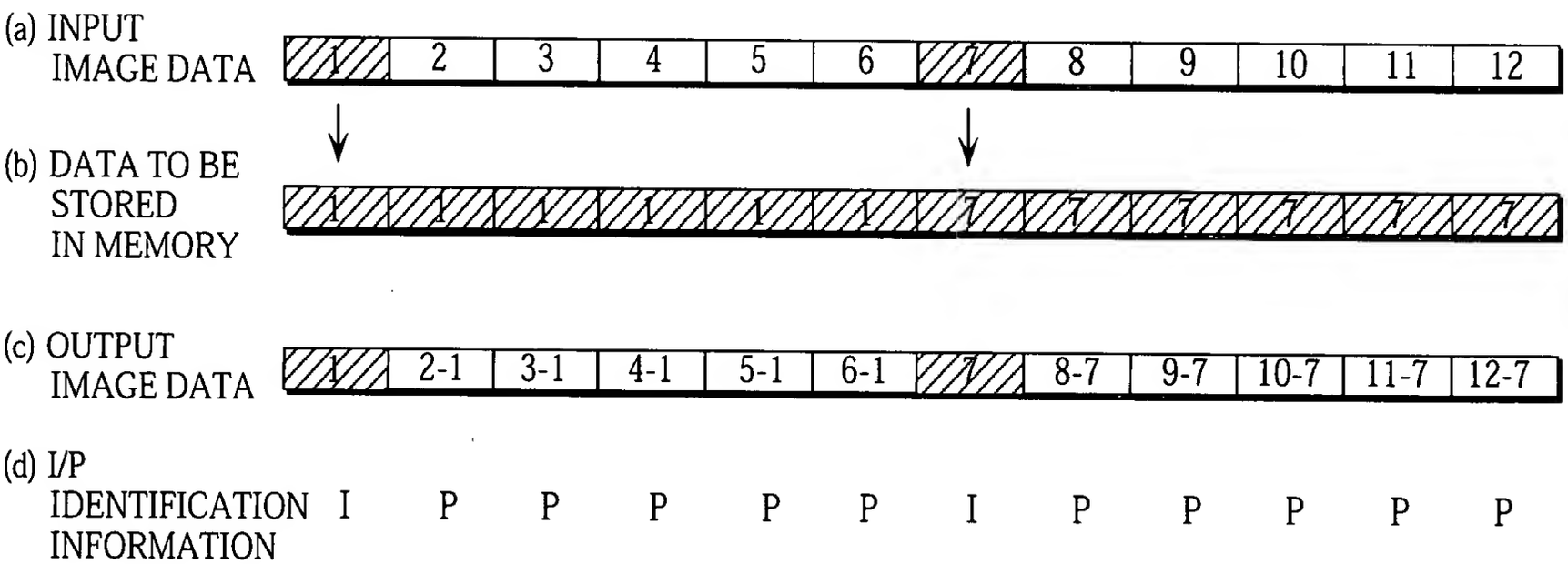

(a) INPUT IMAGE DATA
1
2
3
4
5
6
7
8
9
10
11
12
(b) DATA TO BE STORED IN MEMORY
(c) OUTPUT IMAGE DATA
1
2-1
3-1
4-1
5-1
6-1
7
8-7
9-7
10-7
11-7
12-7
(d) I/P IDENTIFICATION INFORMATION
I P P P P P I P P P P P

FIG. 4

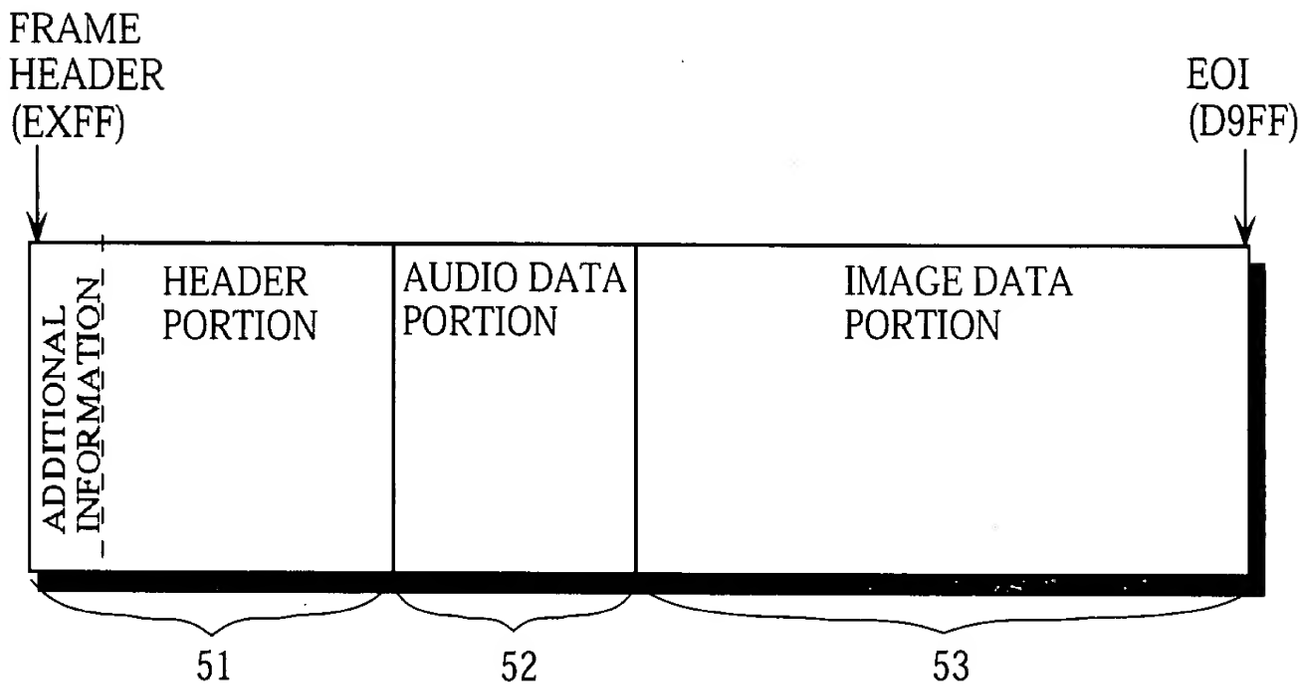

FRAME
HEADER
(EXFF)
EOI
(D9FF)
ADDITIONAL INFORMATION
HEADER PORTION
AUDIO DATA PORTION
IMAGE DATA PORTION
51
52
53

FIG. 5

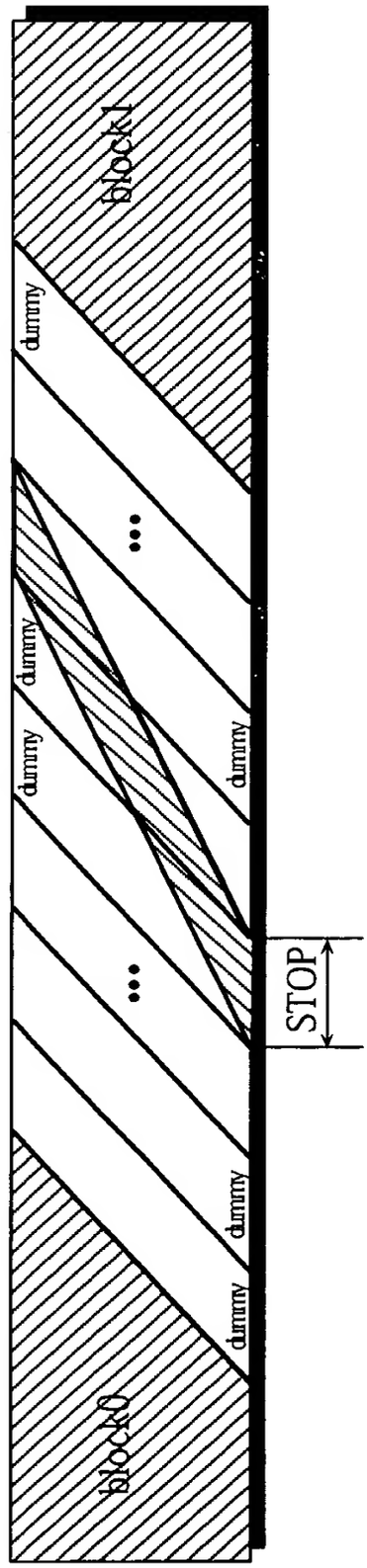

block1
dummy
dummy
dummy
dummy
STOP
dummy
dummy
dummy
block0

FIG. 6

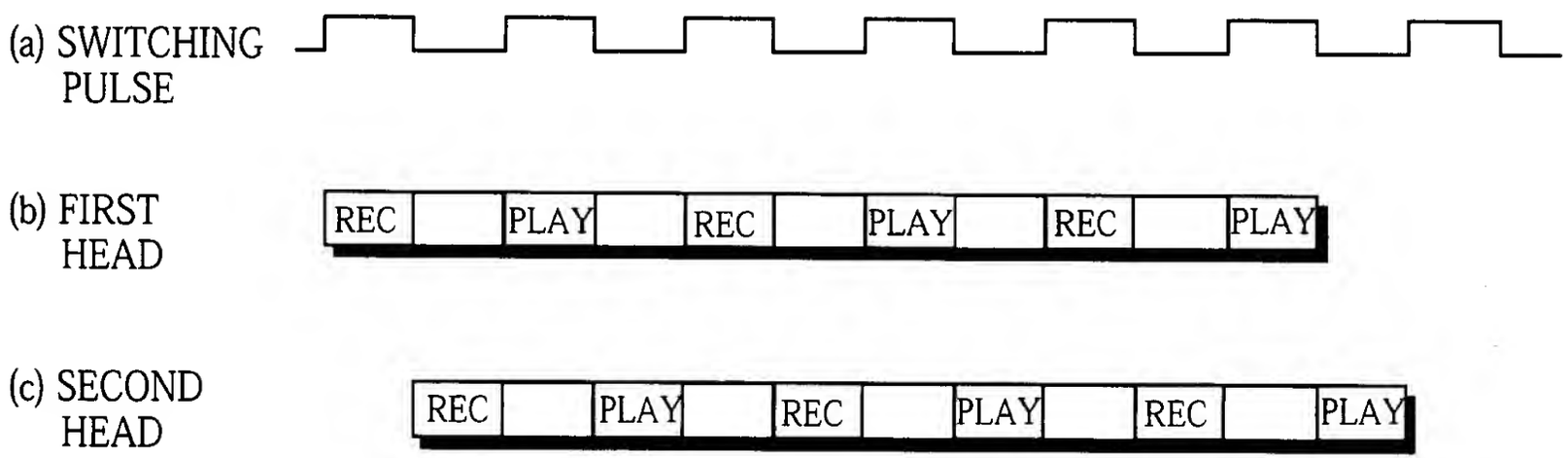

(a) SWITCHING PULSE
(b) FIRST HEAD
REC
PLAY
REC
PLAY
REC
PLAY
(c) SECOND HEAD
REC
PLAY
REC
PLAY
REC
PLAY

FIG. 7

INDEX	ADDRESS IN WHICH FRAME HEADER IS STORED
1	xxxxh
2	xxxxh
3	xxxxh
4	xxxxh
	xxxxh
	xxxxh
	xxxxh
	xxxxh
	xxxxh
	xxxxh
2024	xxxxh

FIG. 8

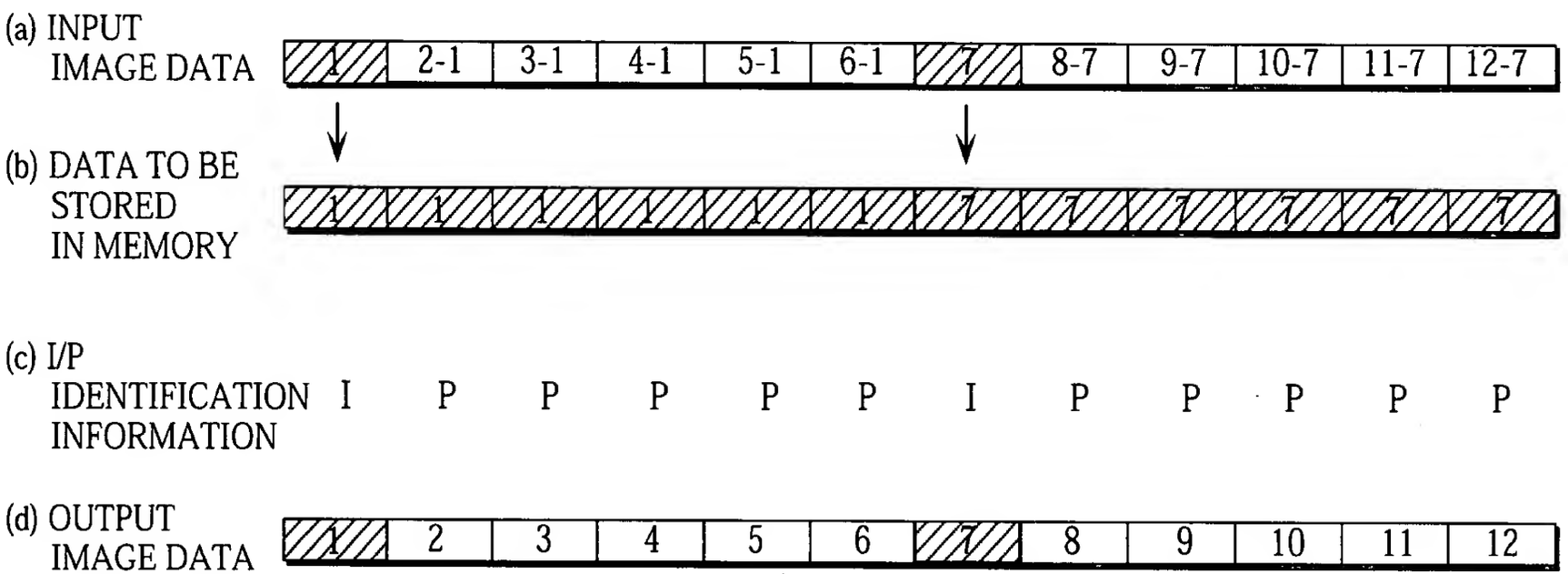

(a) INPUT IMAGE DATA
1
2-1
3-1
4-1
5-1
6-1
7
8-7
9-7
10-7
11-7
12-7
(b) DATA TO BE STORED IN MEMORY
1
1
1
1
1
1
7
7
7
7
7
7
(c) I/P IDENTIFICATION INFORMATION
I P P P P P I P P P P P
(d) OUTPUT IMAGE DATA
1
2
3
4
5
6
7
8
9
10
11
12

FIG. 9

INDEX NUMBER IN SUB-BANK	STORED DATA
1	I1
2	P11
3	P12
4	P13
5	I2
6	P21
7	P22
8	P23
9	I3
10	P31
11	P32
12	P33

FIG. 10

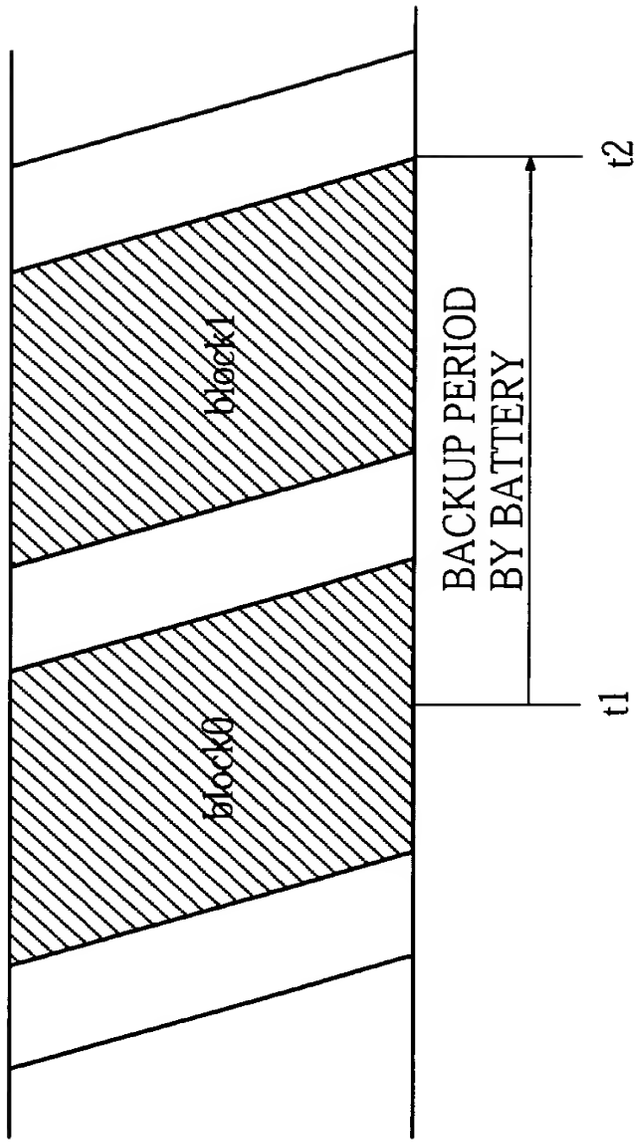


FIG. 11

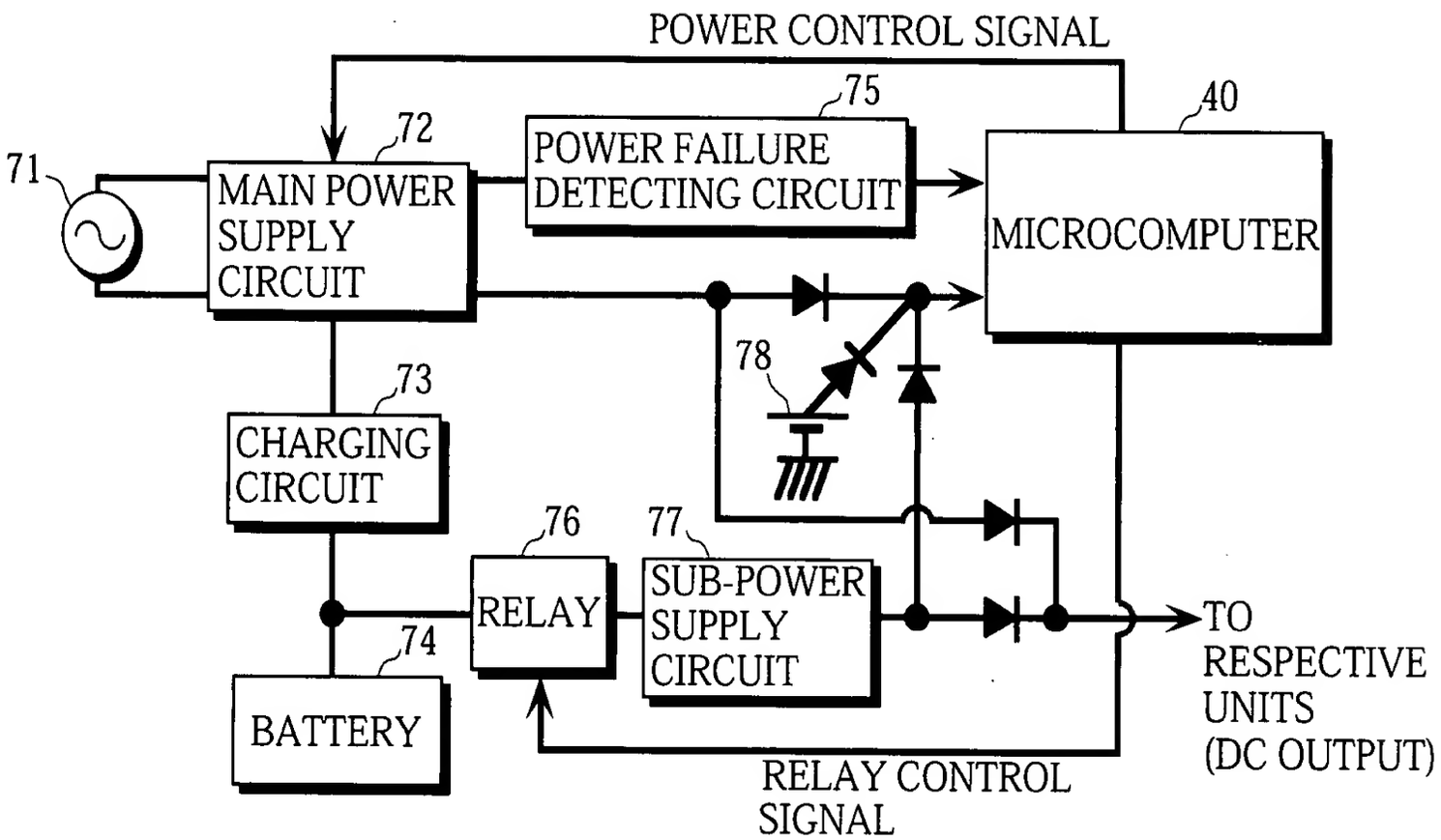
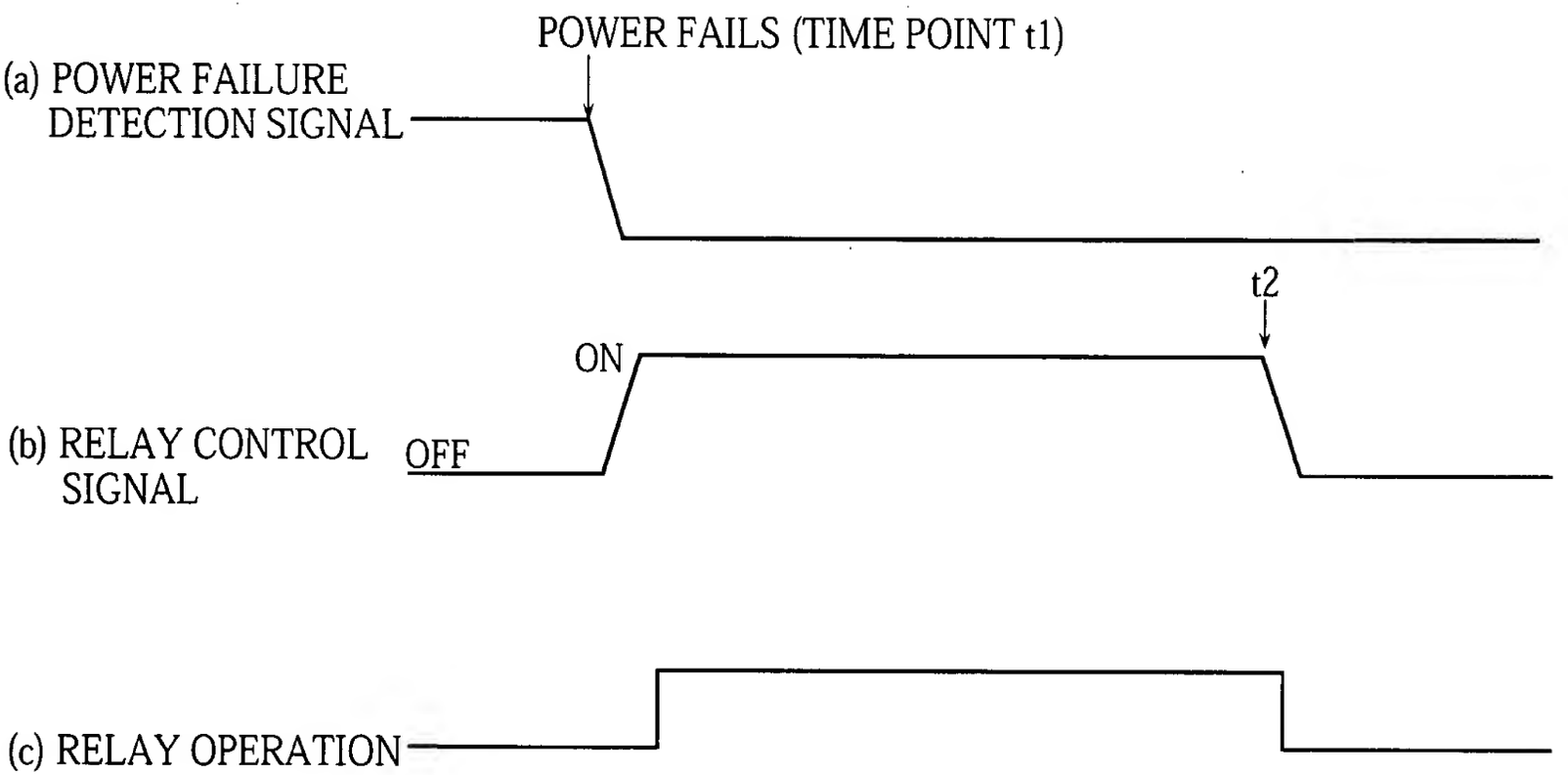

POWER CONTROL SIGNAL
71
72
MAIN POWER SUPPLY CIRCUIT
75
POWER FAILURE DETECTING CIRCUIT
40
MICROCOMPUTER
78
73
CHARGING CIRCUIT
76
77
RELAY
SUB-POWER SUPPLY CIRCUIT
74
BATTERY
TO RESPECTIVE UNITS (DC OUTPUT)
RELAY CONTROL SIGNAL

FIG. 12


POWER FAILS (TIME POINT t1)
(a) POWER FAILURE DETECTION SIGNAL
t2
ON
(b) RELAY CONTROL SIGNAL
OFF
(c) RELAY OPERATION